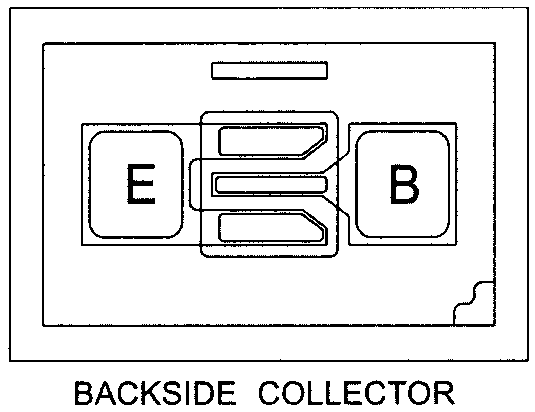
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.014”**



**.009”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0027” X .0027”**

**Backside Potential: Collector**

**Mask Ref: CP207**

**APPROVED BY: DK DIE SIZE .009” X .014” DATE: 1/17/23**

**MFG: CENTRAL SEMI THICKNESS .008” P/N: 2N2369A**

**DG 10.1.2**

#### Rev B, 7/19/02